

What is claimed is:

1           1.     A computer system comprising:  
2           a local bus;  
3           a memory bus capable of indicating data; and  
4           a buffer adapted to capture the data directly from the memory bus, the buffer being  
5 ~~B~~ located closer to the local bus than to the memory bus.

1           2.     The computer system of claim 1, wherein  
2           the memory bus is capable of indicating a data strobe signal, and  
3           the buffer is adapted to latch the data from the memory bus in response to the data strobe  
4           signal.

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1           3.     ~~The computer system of claim 1, further comprising:~~  
2           ~~conductive traces adapted to communicate indications of the data from a first region near~~  
3           ~~the memory bus to a second region near the buffer, the conductive lines introducing an~~  
4           ~~approximate first asynchronous propagation delay in the communication.~~

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1           4.     The computer system of claim 3, further comprising:  
2           circuitry adapted to transfer the data from the buffer to the local bus without introducing a  
3           second propagation asynchronous propagation delay that is greater than the first asynchronous  
4           propagation delay.

1           5.     The computer system of claim 1, wherein the buffer is part of a local bus  
2           interface.

1           6.     The computer system of claim 1, further comprising:  
2           circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of  
3           the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data  
4           without introducing an asynchronous propagation delay greater than approximately one cycle of  
5           the clock signal.

1           7.     The computer system of claim 1, wherein the buffer is part of a local bus interface  
2 that is coupled to the local bus, the computer system further comprising:  
3         a third bus;  
4         a fourth bus;  
5         a third bus interface coupled to communicate with the third bus;  
6         a fourth bus interface coupled to communicate with the fourth bus; and  
7         a multiplexing circuit adapted to selectively cause the buffer to store other data from the  
8 third and fourth bus interfaces.

1           8.     The computer system of claim 1, wherein the buffer is part of a local bus interface  
2 that is located closer to the local bus than to the memory bus.

1           9.     The computer system of claim 8, wherein the local bus interface further  
2 comprises:  
3         a local bus controller adapted to use the buffer to furnish signals to the local bus that  
4 indicate the data.

1           10.    The computer system of claim 1, further comprising:  
2         a memory interface located closer to the memory bus than to the local bus, the memory  
3 interface including another buffer to store other data to be furnished to the memory bus.

1           11.    A bridge for use with a local bus and a memory bus capable of indicating data,  
2 comprising:  
3         conductive traces adapted to communicate indications of the data from a first region near  
4 the memory bus to a second region near the local bus; and  
5         a local bus interface being located closer to the local bus than to the memory bus, the  
6 local bus interface including a buffer adapted to capture the indications of the data from the  
7 conductive traces near the second region to directly capture the data from the memory bus.

1 12. The bridge of claim 11, wherein  
2 the memory bus is capable of indicating a data strobe signal, and  
3 the buffer is adapted to latch the data in response to the data strobe signal.

1 13. The bridge of claim 11, wherein the conductive traces introduce a first  
2 asynchronous propagation delay to the indications of the data, the bridge further comprising:  
3 circuitry adapted to transfer the data from the buffer to the local bus without introducing a  
4 second asynchronous propagation delay that is greater than the first asynchronous propagation  
5 delay.

1 14. The bridge of claim 13, further comprising:  
2 circuitry adapted to transfer the data from the buffer to the local bus, at least a portion of  
3 the circuitry being synchronized to a clock signal and the circuitry adapted to transfer the data  
4 without introducing an asynchronous propagation delay greater than approximately one cycle of  
5 the clock signal.

1 15. The bridge of claim 12, further comprising:  
2 a third bus;  
3 a fourth bus;  
4 a third bus interface coupled to communicate with the third bus;  
5 a fourth bus interface coupled to communicate with the fourth bus; and  
6 a multiplexing circuit adapted to selectively cause the buffer to store other data from the  
7 third and fourth bus interfaces.

1 16. The bridge of claim 12, wherein the local bus interface further comprises:  
2 a local bus controller adapted to use the buffer to furnish signals to the local bus that  
3 indicate the data.

1 17. The bridge of claim 12, further comprising:  
2 a memory interface located spatially closer to the memory bus than to the local bus, the  
3 memory interface including another buffer to store other data to be furnished to the memory bus.

1 18. A method usable with a computer system that includes a local bus and a memory  
2 bus, the method comprising:  
3 furnishing data to the memory bus in a memory read operation; and  
4 capturing the data directly from the memory bus in a buffer that is located closer to the  
5 local bus than to the memory bus.

1 19. The method of claim 18, wherein the act of capturing comprises:  
2 latching the data from the memory bus in response to a data strobe signal of the memory  
3 bus.

1 20. The method of claim 18, further comprising:  
2 using conductive traces adapted to communicate indications of the data from a first  
3 region near the memory bus to a second region near the buffer, the conductive lines introducing  
4 an approximate first asynchronous propagation delay in the communication.

1 21. The method of claim 20, further comprising:  
2 transferring the data from the buffer to the local bus without introducing a second  
3 asynchronous propagation delay that is greater than the first asynchronous propagation delay.

1 22. A method usable with a computer system, comprising:  
2 substantially extending a memory bus into a bridge, the memory bus being adapted to  
3 indicate data in a memory read operation; and  
4 capturing the data directly from the extension of the memory bus into the bridge.

1 23. The method of claim 22, wherein the act of capturing comprises:  
2 latching the data from the extension of the memory bus in response to a data strobe signal  
3 of the memory bus.

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24. The method of claim 22, further comprising:

using conductive traces adapted to communicate indications of the data from a first region near the memory bus to a second region near the buffer, the conductive lines introducing an approximate first asynchronous propagation delay in the communication.

25. The method of claim 24, further comprising:

transferring the data from the buffer to a local bus without introducing a second asynchronous propagation delay that is greater than the first asynchronous propagation delay.

26. The method of claim 22, wherein the act of extending comprises:

extending the memory bus into the bridge so that the extended end of the memory bus is closer to a local bus than to the portion of the memory bus that is located outside of the bridge.

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